Bias Voltage DAC operating at cryogenic Temperatures for Solid-State Qubit Applications

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***Abstract*—A scalable eight channel DAC designed in a TSMC 65nm CMOS technology for generation of solid-state quantum bit (qubit) bias voltages is presented. Measurement results of the DAC and some additional auxiliary components like an on-chip amplifier and Sigma-Delta modulator at 6 K are discussed. With a low power consumption of 2.7 µW per channel, the DAC fulfills the requirements to be placed next to qubits inside a mixing chamber of a dilution refrigerator, showing a promising way for scaling qubit numbers towards a quantum computer.**

***Index Terms*—CMOS, cryogenic, DAC, qubit, quantum computing**

I. Introduction

One of the promises of quantum computing is to perform certain tasks up to exponentially faster than a classical computer. Examples of the applications are quantum chemistry (e.g. catalyst research and protein folding) followed by search algorithms for unordered databases to cryptography (e.g. prime factorization) [1].

A prominent aspect in current research is scaling up the number of used qubits, like Google recently presented the operation of 53 qubits in their Sycamore processor [2]. One promising approach for further upscaling the control and readout electronics lies in utilizing modern CMOS technologies close to the qubits to overcome limitations when feeding an increasing number of lines into the cryostat. Compared to discrete electronics, the benefits of ICs are: smallest form factor, lowest power consumption, high performance and best efficiency when tailored to the application. All aspects bringing clear advantages to cope with the low area demand and power consumption inside a dilution refrigerator. It is already proven that CMOS circuits can operate at deep cryogenic temperatures [3]. However, only few cryogenic DACs are reported so far, see Table III.

Therefore, as a first prototype chip for integrated qubit control a specially designed IC was developed to be used at temperatures of 100 mK to bias GaAs spin-based qubits. Fig. 1 shows a block level overview of the two Bias DACs, one to connect to the qubit and a duplicate wired to the auxiliary circuits for measurement purposes.Grey blocks are turned off when biasing the qubit. Section II describes the application and the specific requirements. The following section III describes the multi-channel-output DAC. Section IV shows measurement results at cryogenic temperatures of approx. 6 K.

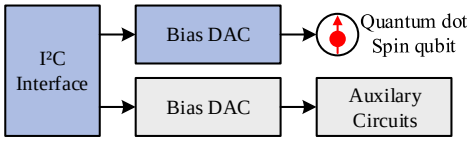


Fig. 1. Block diagram of Bias DACs connectivity.

II. Application

Solid-state qubits have to be operated at cryogenic temperatures below liquid helium (4.2 K), commonly around 100 mK, to maximize coherence and dephasing times. Such low temperatures can be reached by dilution refrigerators. The typical cooling power of nowadays dilution refrigerators at 100 mK is around 400 µW [4].

The requirements presented here are specific to GaAs and SiGe solid-state spin-based qubits [1]. These qubits are created by forming a quantum dot and trapping one or multiple electrons to build a qubit utilizing the quantum mechanical properties of electron spins. The Bias DAC is designed to supply up to 8 independent voltages simultaneously with a range of 0 V to 1 V and a step size of about 125 µV, i.e. 13 bit resolution, including a margin for the required 12 bit of the qubit, see Table I. The total power consumption should be kept well below 1 mW to prevent extremely heating up the dilution refrigerator, at best below the mentioned 400 µW. The design considers all aspects for future scalability and is therefore optimized with respect to duplicating the DAC many times for biasing a high number of qubits.

TABLE I
Requirements for GaAs Qubit Bias Voltages

Parameter	Specification
Voltage range	0 V to 1 V
Stepsize	250 µV (≈ 12 bit)
Temperature	100 mK
Power	≪ 1 mW

III. Bias DAC

As circuit topology for the Bias DAC a charge-redistribution structure was chosen, as shown in Fig. 2.This topology has application specific advantages, e.g. no static power dissipation and bandwidth independent Johnson–Nyquist noise of $\overline{v_n^2} = \frac{k_B T}{C}$. Changes in capacitor properties, due to temperature decrease, are reported to be small [5]. Multiple output channels are created by demultiplexing the output of the DAC to various Sample and Hold (S&H) structures. The typically present output buffer is removed to minimize power, area and noise, since it is not required to charge the capacitor of the S&H in a single conversion step. The voltage on the storage capacitor $C_{Storage}$ increases in discrete steps each time the DAC drives the specific output channel.

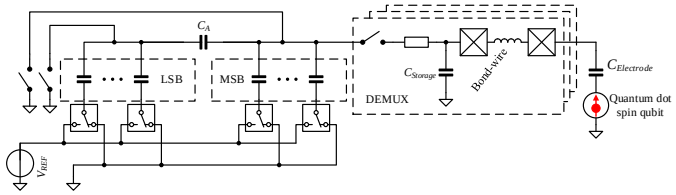
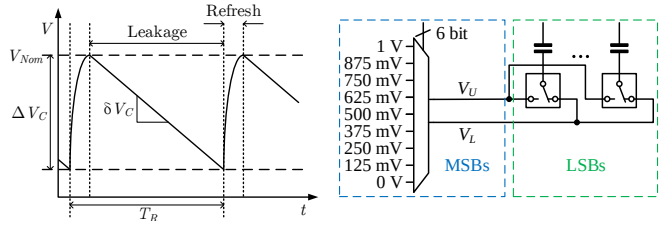


Fig. 2. Charge-redistribution DAC.

A periodical refresh of each output channel is necessary because of possible leakage currents or distortions at the S&H capacitor. Voltage changes due to these effects should be minimized and ideally stay in the lower tens of microvolt. This periodical refreshing of each output channel is leading to a voltage behavior due to leakage as is shown in Fig. 3a.



(a) Periodical refresh. (b) Coarse tuning.

Fig. 3. Compensation of leakage by periodical refresh and independently coarse tune upper and lower reference voltages.

Simulations showed capacitance mismatch is posing a limit to go beyond about 10 bit of resolution without adding calibration. In [6] the effect of mismatch to DNL for the binary-weighted capacitive array with attenuation capacitor (BWA) is derived as:

$$\sigma^2_{DNL,BWA} = \sigma^2_D \approx 2^{\frac{3N}{2}} \cdot \left(\frac{\sigma_0}{C_0}\right)^2 \text{LSB}^2 \qquad (1)$$

Multiplexing of 8 different external reference voltages to gain additional 3 bit of resolution, reaching the specified resolution of 12 bit, is proposed, as shown in Fig. 3b. Tuning the reference voltages results in a reduction from 1 V to 0.125 V charging the DAC capacitors. By $P \propto V^2 \cdot f \cdot C$, lowering the power consumption with a factor of $(1/8)^2 = 1/64$.

A. Measurement Auxiliary Circuits

Due to the low driving strength of the DAC, intentionally only designed to counteract leakage currents of pA, some additional circuitry was added to the IC enabling measurement of the DAC, shown in Fig. 4. First, 3 different Operational Amplifier (OpAmp) configurations are included, see Fig. 5. Additionally, a $\Sigma\Delta$-modulator was designed to employ on-chip analog-to-digital conversion in case the cabling or other noise sources (e.g. crosstalk of the long twisted-pair cables inside the dilution refrigerator) impose a problem to measure via the amplifiers. For later debugging, the same OpAmp is used for the integrators in the $\Sigma\Delta$-modulator. By filtering the bitstream output of the modulator, which is done digitally at room temperature, the averaged DC voltage level should be measurable. In addition, a window comparator (WC) is included to detect drifts of this voltage.

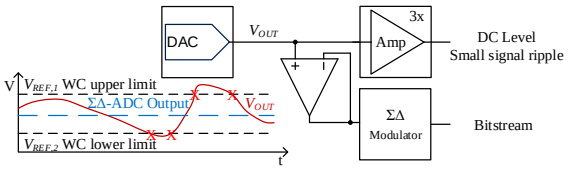


Fig. 4. On-chip auxiliary circuits enabling measurement of the Bias DAC.

The OpAmp topology used for the three configurations is a Miller-OpAmp, as shown in Fig. 5. M3 and M4 are used as a PMOS input differential stage, transistors M5 to M7 are designed as a cascode current mirror load. M11 and M12 are used as a class A output stage. R1 and C1 are used as dominant pole for stabilization. OpAmp configurations were included for test case purposes, enabling additional on-chip gain and optional voltage to current conversion for upcoming noise (mainly refresh, ref. to Fig. 3a) measurements.

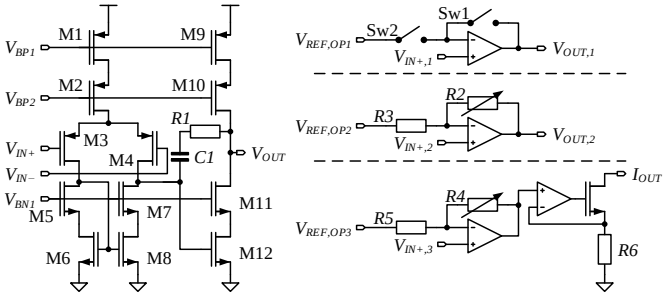


Fig. 5. The OpAmp design and three different configurations present on-chip.

IV. Measurement

Measurement was performed inside an Attocube attoDRY800 closed-cycle helium cryostat, which reaches base temperatures of about 6 K.

A. Operational Amplifier

The OpAmp shows an open loop gain of 70 dB for both cryogenic (cryo) and room temperature (RT). The measured

offset voltage shift of about 2 mV is still in the range of process mismatch. However, when operated as unity gain buffer a clipping is apparent for input voltages higher than 700 mV, as shown in Fig. 6. The input common-mode voltage of the OpAmp is increasing above the threshold voltage of the input PMOS pair M3 and M4 in Fig. 5, the steep subthreshold slope at cryogenic temperatures renders an operation in moderate or weak inversion unfeasible. An increase by ΔV_{DD} would shift the point of clipping by the same amount upwards. As the OpAmp is biased by an externally fed reference current, the power consumption is about the same for cryo (1.2 V: 120 µW, 1.7 V: 270 µW) and RT (1.2 V: 140 µW, 1.7 V: 240 µW). Unity gain bandwidth was measured with cabling load ($\approx$ 100 pF, no active probing possible due to cryostat setup) and shows a slight increase from 225 kHz at RT to 250 kHz at 6 K. The output voltage range is limited close to the ground rail, resulting in an output voltage of 54 mV at 0 V input for RT, which decreases to 33 mV at 6 K. An explanation is increased mobility requiring less drain source voltage V_{DS} for the equal amount of drain current. Hence, showing a fully functional OpAmp at temperatures down to approx. 6 K.

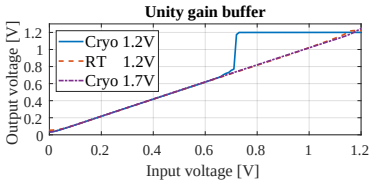


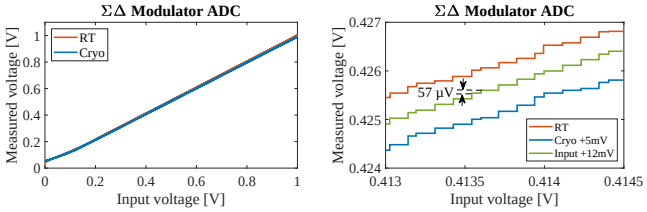
Fig. 6. Unity gain buffer sweep at RT and inside cryostat at 6 K.

B. ΣΔ Modulator

The ΣΔ Modulator requires the same supply voltage increase to 1.7 V as its internal circuitry is based on the previously described OpAmp and a track and latch comparator structure. The common-mode feedback (CMFB) voltage regulation of the (PMOS input pair) differential amplifier of the comparator is also set to lower values at cryogenic temperatures to avoid clipping effects. Fig. 7 shows the digitally filtered output of the ΣΔ-modulator for an input voltage sweep (RT measurement equipment, 100 µV steps programmed, some steps are as small as 57 µV and not induced by the ΣΔ). Both with a supply voltage of 1.7 V and similar reference current settings. At cryogenic temperatures the CMFB voltage setting was lowered from 700 mV to 500 mV leaving enough margin for the comparators to operate. Power consumption is in the range of about 1 mW. The offset in Fig. 7b poses no issue and can easily be subtracted. This offset shift by 5 mV due to temperature change is consistent with the change expected due to offset shift in amplifier and comparator circuits. Voltages close to ground are again limited by the finite output voltage range of the OpAmps. The ΣΔ-modulator shows similar performance for RT and deep cryogenic temperatures.

C. Bias DAC

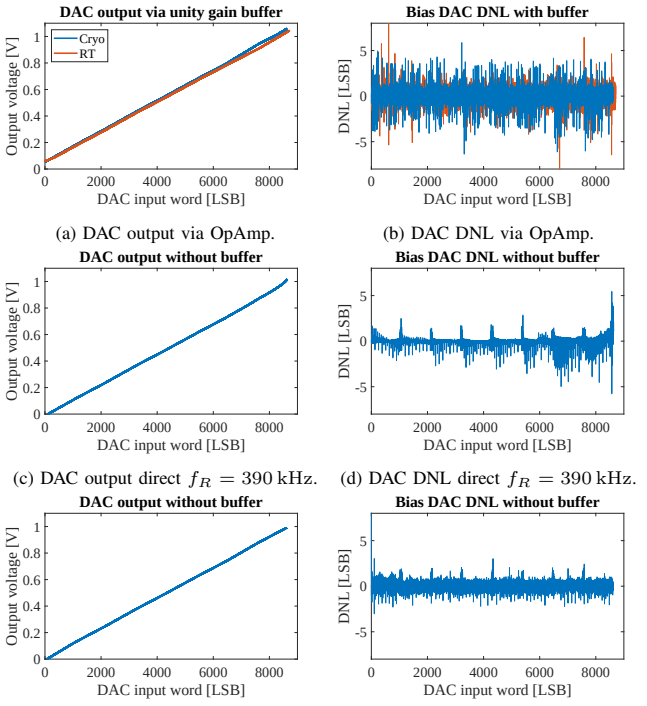
The Bias DAC was measured via an on-chip unity gain buffer and directly. The latter was possible by setting the



(a) Full scale. (b) Zoomed & shifted to fit plot.

Fig. 7. ΣΔ modulator filtered output over input voltage sweep.

Keysight 34470A multimeter to an input load of 10 GΩ instead of 10 MΩ default. Measuring via the unity gain buffer the voltage supply was increased to 1.7 V to measure the full output range of the Bias DAC 0 V to 1 V as discussed in section IV-A. Results for the nominal channel refresh rate $f_R = 1/T_R = 390$ kHz (ref. to Fig. 3a) are shown in Fig. 8a and 8b. For getting these results one negative aspect of using reference voltage coarse tuning (ref. to Fig. 3b) had to be mitigated. Parasitic capacitance induces a gain error, creating a jump when switching coarse tuning regions, see Fig. 9a. Intermediate steps can be added to fill the missing output range by not directly going to the next 125 mV coarse tuning setting but rather add some steps by operating with 250 mV coarse tuning setting, see Fig. 3b showing upper V_U and lower V_L reference voltages. Comparing direct and via unity-gain buffer measurements, a noticeable difference in DNL is visible, which indicates a non-negligible influence of the unity gain buffer. Moreover, a repeating pattern is visible for each

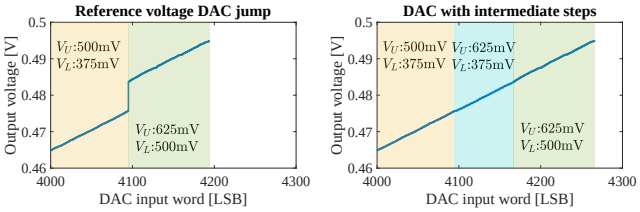


(a) DAC output via OpAmp. (b) DAC DNL via OpAmp.

(c) DAC output direct $f_R = 390$ kHz. (d) DAC DNL direct $f_R = 390$ kHz.

(e) DAC output direct $f_R = 3.9$ kHz. (f) DAC DNL direct $f_R = 3.9$ kHz.

Fig. 8. Output of Bias DAC at channel refresh rate $f_R = 390$ kHz for Fig. 8a to 8d and $f_R = 3.9$ kHz for Fig. 8e to 8f. Legend of Fig. 8a apply to all graphs.



(a) Coarse tuning induced jumps.

(b) Fill missing output range with double the stepsize.

Fig. 9. Reference voltage coarse tuning effect and mitigation.

10 bit word (1023 LSBs) as this is the range of the DAC without switching reference voltages, see Fig. 8d. Measurements showed a sweet spot for power and performance at a channel refresh rate of 3.9 kHz, output voltage and corresponding DNL are shown in Fig. 8e and 8f, measured directly without any buffer. Substituting the measured $\sigma_D = 0.495\,\text{LSB}$ in (1) yields a capacitor mismatch of $\sigma_0 = 0.003\,C_0$. For all shown measurements in this section all eight channels of the Bias DAC were active and running. The power consumption of the Bias DAC at cryogenic temperatures is listed in Table II. 99.5 % of the Bias DAC power is dissipated in digital circuitry and scales well with CMOS technology node. Furthermore, it is not required to duplicate all of the digital blocks with each additional Bias DAC, because timing signals controlling the DAC can be generated only once on-chip and distributed to all Bias DACs, e.g. opening the reset or S&H switches, see Fig. 2. Only some digital memory circuitry is required for each individual DAC. A die photograph of the prototype chip is shown in Fig. 10. The DAC is compared with other cryogenic DACs in Table III and is filling the missing gap of an ultra-low power multi-channel DAC operating at cryogenic temperatures down to 6 K.

TABLE II
DAC POWER CONSUMPTION FOR $f_R = 3.9\,\text{kHz}$

Block	Power consumption
DAC core (Sw&MUX: Fig. 2&3b)	77 nW
DAC reference voltages (Fig. 3b)	3 nW
DAC digital (memory & logic)	21 µW
DAC total	21.1 µW (2.63 µW per channel)
Clock buffer	4.3 µW
Total	25.4 µW (3.18 µW per channel)

V. CONCLUSION

An eight channel DAC operating at cryogenic temperatures of about 6 K was shown enabling a scalable solution for qubit biasing with an output voltage range of 1 V, consuming about 2.7 µW per channel, 99.5 % in digital logic and memory, which scales well with CMOS technologies nodes. A total chip power consumption of well below 400 µW (including I^2C, and other non-active blocks on the chip) allows for placement of the DAC inside the mixing-chamber of a dilution refrigerator and directly bondwire to the qubit chip. This is also the next step to show a promising scalable solution for qubit scaling by utilizing modern CMOS technologies.

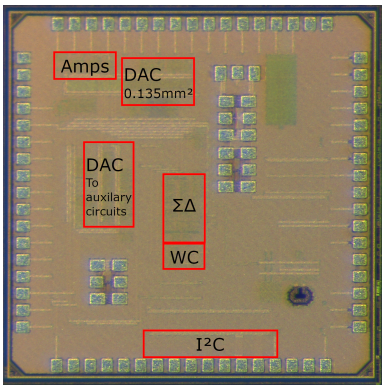


Fig. 10. Die photograph of the prototype chip.

TABLE III
COMPARISON WITH OTHER CRYOGENIC DACS.

	[7]	[8]	[9]	this work
Technology	0.5 µm SiGe BiCMOS	0.5 µm SiGe BiCMOS	0.5 µm SOS BiCMOS	65 nm CMOS
Temperature	93.15 K	93.15 K	4.2 K	6 K
Type	Current steering	Current steering	Current steering	Charge-redistribution
Resolution	12 bit	8 bit	10 bit	13 bit
Channel	1	1	1	8
Power	39.6 mW	3 mW	32.18 mW	21.1 µW
Supply	3.3 V	3.3 V	3 V	1.2&2.5 V
Area	6.3 mm^2	0.25 mm^2	1.1 mm^2	0.14 mm^2

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